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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/879,725	06/12/2001	Neil Clair Berglund	ROC920010019US1	4894

7590 09/21/2004

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EXAMINER	
BUTLER, DENNIS	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 09/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/879,725	BERGLUND ET AL.	
	Examiner	Art Unit	
	Dennis M. Butler	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 June 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/12/01, 10/20/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. This action is in response to the application filed on June 12, 2001. Claims 1-26 are pending.

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1, 3 and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Taroda et al., U. S. Patent 5,724,542.

Per claim 1 and 13:

A) Taroda et al teach the following claimed items:

1. apparatus performing power fault analysis including a control device (power unit controller 39a and BTU 39c) with figure 22;

2. an information circuit having a non-volatile memory field for storing a state variable with the memory circuitry of BTU 39c of figure 22 and at column 20, lines 27-32;

3. the state variable (OFF OK) assuming a first state when the computer is powered on and operating with figure 23, at column 20, lines 27-32 and at column 22, lines 1-8;

4. the state variable (OFF OK) assuming a second state when the computer is powered off in response to a power off request at column 20, line 61 – column 21, line 41;

5. the control device (power unit controller 39a and BTU 39c) reading the state variable (OFF OK) from the information circuit at column 20, lines 33-53.

Per claim 3:

Taroda describes that the information circuit includes a memory consisting of PROM or NVRAM or CMOS or flash memory with figure 23, at column 20, lines 27-32 and at column 21, lines 58-67. Taroda describes that the information circuit stores the state values when both of the power supplies are off and describes BTU 39c having battery back-up.

6. Claims 2, 6, 8, 10, 12, 16, 19 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taroda et al., U. S. Patent 5,724,542 in view of Berglund et al., U. S. Patent 6,055,581.

Per claims 2, 6, 8, 10, 12, 16, 19 and 21:

Taroda et al teach the elements of claims 1 and 13 as described in the above rejection. The claims seem to differ from Taroda et al in that Taroda et al fails to explicitly teach using a VPD circuit for the information circuit, the system having a CEC frame and a I/O frame coupled by a SPCN and the CEC and I/O frames maintaining error logs as claimed. Berglund teaches that it is known to use a VPD circuit for storing state information in a system having a CEC frame and an I/O frame coupled by a SPCN at column 1, line 47 – column 2, line 10. It would have been obvious to one having ordinary skill in the art at the time the invention was made to use a VPD circuit for storing state information in a system having a CEC frame and a I/O frame coupled by a SPCN, as taught by Berglund, in order to store power state information for determining whether the system powered of in response to a power-off request. One of ordinary skill in the art would have been motivated to combine Taroda and Berglund because of Berglund's suggestion of adding VPD chips to a computer system to store asset information at column 2, lines 1-10. It would have been obvious for one of ordinary skill in the art to combine Taroda and Berglund because they are both directed to the problem of monitoring and storing power information. Regarding the error logs, error logs are well known in the data processing art and it would have been obvious to include error logs in order to record and track power failures in the system.

7. Claims 4, 5, 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taroda et al., U. S. Patent 5,724,542 in view of Mermelstein, U. S. Patent 6,052,793.

Per claims 4, 5, 14 and 15:

Taroda et al teach the elements of claims 1 and 13 as described in the above rejection. In addition, Taroda teaches powering down UPC 39a of figure 22 when utility power is removed due to a disturbance at column 21, lines 58-67. The claims seem to differ from Taroda et al in that Taroda et al fails to explicitly teach reading the state variable upon powering up the portion of the control device and operating the control device in a standby mode when the system is powered off. Mermelstein teaches that it is known to read a state variable upon powering up a portion of a control device and operating the control device in a standby (sleep) mode when the system is powered off with figures 1 and 2, at column 1, lines 27-65 and at column 4, line 56 – column 5, line 6. It would have been obvious to one having ordinary skill in the art at the time the invention was made to read a state variable upon powering up a portion of a control device and operating the control device in a standby (sleep) mode when the system is powered off, as taught by Mermelstein, in order to determine whether the system is powering up in response to a power fault event and in order to reduce power consumption. One of ordinary skill in the art would have been motivated to combine Taroda and Mermelstein because of Mermelstein's suggestion of having the BIOS determine whether the system is booting in response to an invalid event or power failure at

column 4, line 65 – column 5, line 6. It would have been obvious for one of ordinary skill in the art to combine Taroda and Mermelstein because they are both directed to the problem of monitoring and storing power information.

8. Claims 7, 9, 11, 17, 18 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taroda et al., U. S. Patent 5,724,542 in view of Johnson et al., U. S. Patent 6,122,758.

Per claims 7, 9, 11, 17, 18 and 20:

Taroda et al teach the elements of claims 1 and 13 as described in the above rejection. The claims seem to differ from Taroda et al in that Taroda et al fails to explicitly teach maintaining an error log of the power information as claimed. Johnson teaches that it is known to maintain an error log of power information with figures 11A through 12, at column 19, line 63 – column 20, line 4 and at column 20, lines 5-16. It would have been obvious to one having ordinary skill in the art at the time the invention was made to maintain an error log of power information, as taught by Johnson, in order to record and track power failures in the system. One of ordinary skill in the art would have been motivated to combine Taroda and Johnson because of Johnson's suggestion recording any change in status of a power supply using a log at column 20, lines 11-16. It would have been obvious for one of ordinary skill in the art to combine Taroda and Johnson because they are both directed to the problem of monitoring and storing power information.

9. Claims 22, 25 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taroda et al., U. S. Patent 5,724,542 in view of IBM TDB "Fault Indicator Software Support for Operational Personal Computer Systems" (cited by applicant).

Per claim 22:

A) Taroda et al teach the following claimed items:

1. apparatus performing power fault analysis including a control device (power unit controller 39a and BTU 39c) with figure 22;

2. an information circuit having a non-volatile memory field for storing a state variable with the memory circuitry of BTU 39c of figure 22 and at column 20, lines 27-32;

3. the state variable (OFF OK) assuming a first state when the computer is powered on and operating with figure 23, at column 20, lines 27-32 and at column 22, lines 1-8;

4. the state variable (OFF OK) assuming a second state when the computer is powered off in response to a power off request at column 20, line 61 – column 21, line 41.

B) The claims seem to differ from Taroda et al in that Taroda et al fails to explicitly teach a program product performing the fault analysis as claimed.

C) However, IBM teaches that it is known to implement power fault analysis systems as a program product as described in the TDB. It would have been obvious to one having ordinary skill in the art at the time the invention was made to implement Taroda's power fault analysis system as a program product, as

suggested by the IBM TDB, in order to increase the flexibility of implementing Taroda's power fault analysis system into various types of data processing systems. One of ordinary skill in the art would have been motivated to combine Taroda and IBM TDB because of IBMs suggestion of providing an interface for languages used by application programmers. It would have been obvious for one of ordinary skill in the art to combine Taroda and IBM TDB because they are both directed to the problem of providing fault indicators for power systems in data processing devices.

Per claims 25 and 26:

Recordable type media and transmission type media are well known media used for storing program products and it would have been obvious to store a program product on such media.

10. Claims 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taroda et al., U. S. Patent 5,724,542 in view of IBM TDB "Fault Indicator Software Support for Operational Personal Computer Systems" (cited by applicant) and further in view of Mermelstein, U. S. Patent 6,052,793.

Per claims 23 and 24:

Taroda et al in view of IBM TDB disclose the elements of claim 22 as described in the above rejection. In addition, Taroda teaches powering down UPC 39a of figure 22 when utility power is removed due to a disturbance at column 21, lines 58-67. The claims seem to differ from Taroda et al in that Taroda et al fails to explicitly teach reading the state variable upon powering up the portion of the

control device and operating the control device in a standby mode when the system is powered off. Mermelstein teaches that it is known to read a state variable upon powering up a portion of a control device and operating the control device in a standby (sleep) mode when the system is powered off with figures 1 and 2, at column 1, lines 27-65 and at column 4, line 56 – column 5, line 6. It would have been obvious to one having ordinary skill in the art at the time the invention was made to read a state variable upon powering up a portion of a control device and operating the control device in a standby (sleep) mode when the system is powered off, as taught by Mermelstein, in order to determine whether the system is powering up in response to a power fault event and in order to reduce power consumption. One of ordinary skill in the art would have been motivated to combine Taroda and Mermelstein because of Mermelstein's suggestion of having the BIOS determine whether the system is booting in response to an invalid event or power failure at column 4, line 65 – column 5, line 6. It would have been obvious for one of ordinary skill in the art to combine Taroda, IBM TDB and Mermelstein because they are directed to the problem of monitoring and storing power information.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dennis M. Butler whose telephone number is 703-305-9663. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Dennis M. Butler

Dennis M. Butler
Primary Examiner
Art Unit 2115